Exhibit L

MacInnis 7,530,027 Applied to Representative Panasonic and Toyota Accused Products

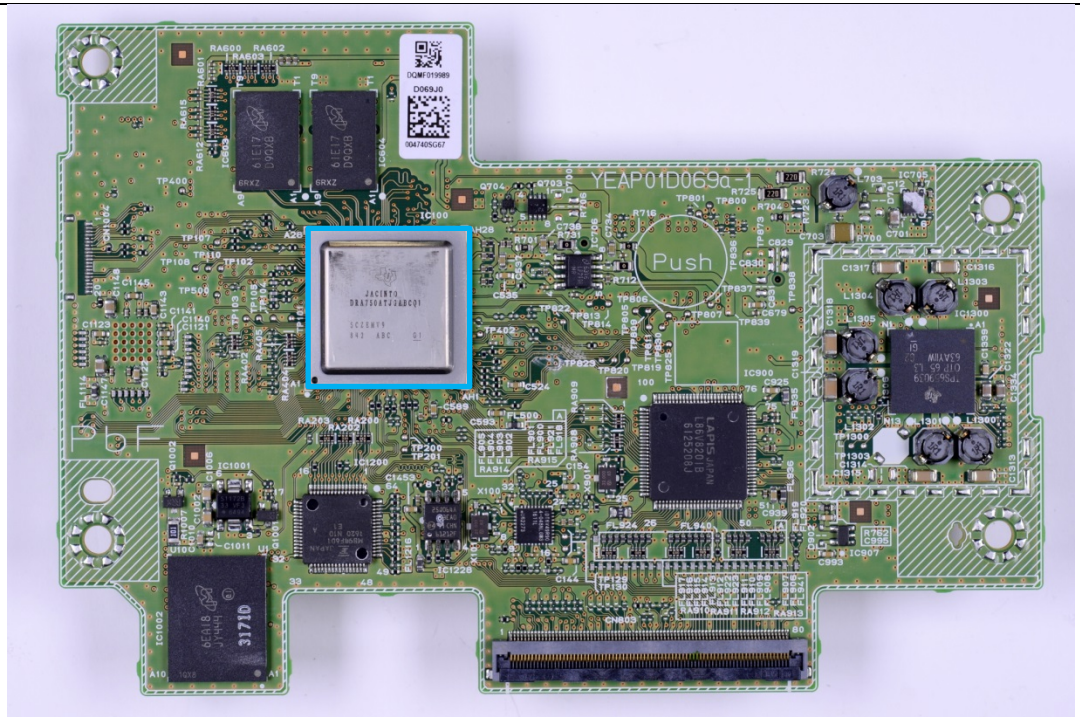
This claim chart compares independent claim 11 of U.S. Patent No. 7,530,027 ("the MacInnis '027 patent") to Texas Instruments' DRA750 system on a chip ("SoC").

On information and belief, Texas Instruments's DRA750 SoC is representative of other Texas Instruments infotainment and high-end car information system SoCs having similar functionality ("Accused Texas Instrument Infotainment SoCs").

The DRA750 SoC is incorporated in downstream products, including without limitation, Panasonic head units, such as Ser. Nos. 130105, 104020, 104069, 500021, which are incorporated in Accused Toyota Navigation units, including Highlander Receiver (86804-0E280), Sienna Navigation Unit (86804-08040), Avalon Navigation Head Unit (86804-07120), and Prius III Navigation System Kit (86804-47330), respectively.

On information and belief the Accused Texas Instrument Infotainment SoCs, and head units and automobiles that incorporate the Accused Texas Instrument Infotainment SoCs infringe directly, indirectly, and or under the doctrine of equivalents, at least claim 11 of the MacInnis '027 patent.

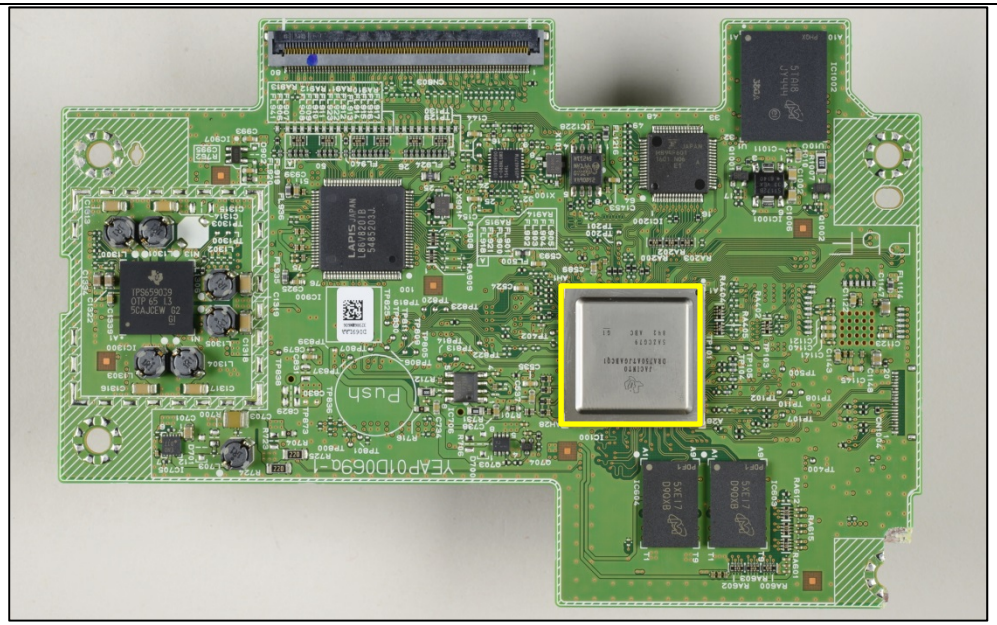
Claim – U.S. Patent No. 7,530,027 (MacInnis)	**Application of Claim Language to Accused Product**
Claim 11	
A system for processing graphics images, comprising:	To the extent that the preamble is deemed limiting, the Accused Texas Instrument Infotainment SoCs and head units and automobiles that incorporate the Accused Texas Instrument Infotainment SoCs comprise a system for processing graphics images. At least the Panasonic Navigation Unit Model No. 86804-47330 incorporates the Texas Instruments DRA750 (highlighted in blue)



The following photograph of the 2017 Toyota Prius III, which includes Panasonic Navigation Unit Model No. 86804-47330, shows the Texas Instruments DRA750 in the Panasonic Navigation Unit Model No. 86804-47330 processing graphics images.[1]

[1] Image from http://autoweek.com/gallery/car-reviews/gallery-2017-toyota-prius-three-interior

	 Additionally, the Panasonic Navigation Unit Model No. 86804-08040 incorporates the Texas Instruments DRA750 (highlighted in yellow).

	 The following photographs of the 2017 Toyota Sienna, which includes Panasonic Navigation Unit Model No. 86804-08040, show the Texas Instruments DRA750 in the Panasonic Navigation Unit Model No. 86804-08040 processing graphics images.

	 
a window controller for obtaining data that describes windows in which the graphics images are displayed, and for sorting the data	The Accused Texas Instrument Infotainment SoCs' and head units and automobiles that incorporate the Accused Texas Instrument Infotainment SoCs' system for processing graphics images comprise a window controller for obtaining data that describes windows in which the graphics images are displayed, and for sorting the data in accordance with respective depths of the windows because they include at least a Display Controller (DISPC) and/or a 2D Graphics Engine (BB2D).

in accordance with respective depths of the windows;

The Technical Reference Manual for the DRA75x SoC for Automotive Infotainment Silicon Revision 2.0, 1.x explains that, in the Display Controller (DISPC), there is an overlay manager which displays more than one layer (GFX, VID1, VID2, and VID3 layers) using, at least, "[a] priority rule based on a Z-order: Application can set the ordering layer of the frames." Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2942.

The Technical Reference Manual further explains that the Z-Order parameter sorts data in accordance with the respective depths of windows.

11.2.4.13.1.1 DISPC Priority Rule

The overlay manager is configured using the Z-order parameter. The Z-order value defined for each pipeline indicates the visibility order to the window on the screen. If the Z-order value of window A is lower than the Z-order to layer B, layer A is displayed below layer B. The transparency color keys and the alpha blending factors are then used to blend the layers together (see Section 11.2.4.13.1.2, *DISPC ALPHA Blender*, and Section 11.2.4.13.1.3, *DISPC Transparency Color Keys*). The Z-order is enabled by setting the DISPC_GFX_ATTRIBUTES[25] ZORDERENABLE bit or the DISPC_VIDp_ATTRIBUTES[25] ZORDERENABLE bit to 0x1 and by defining the Z-order in the DISPC_GFX_ATTRIBUTES[27:26] and DISPC_VIDp_ATTRIBUTES[27:26] ZORDER bit fields. Table 11-112 summarizes the register settings to enable and set the Z-order of a pipeline. Table 11-112 shows the default Z-order values when LCDALPHABLENDERENABLE and ZORDERENABLE are disabled.

Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2943 (highlighted).

Table 11-112. DISPC Z-Order Register Settings and Default Configuration

Pipeline	LCDALPHA BLENDERENABLE[1]	ZORDERENABLE	ZORDER	Resulting Z-Order Number
GFX	0	0	Don't care	0
	0	1	ZORDER	ZORDER
	1	Don't care	Don't care	3
VID1	0	0	Don't care	1
	0	1	ZORDER	ZORDER
	1	Don't care	Don't care	0

Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Table 11-112 at 2943.

The Technical Reference Manual states that the Z-order is enabled by setting registers.

11.2.4.13.1.1 DISPC Priority Rule

The overlay manager is configured using the Z-order parameter. The Z-order value defined for each pipeline indicates the visibility order to the window on the screen. If the Z-order value of window A is lower than the Z-order to layer B, layer A is displayed below layer B. The transparency color keys and the alpha blending factors are then used to blend the layers together (see Section 11.2.4.13.1.2, *DISPC ALPHA Blender*, and Section 11.2.4.13.1.3, *DISPC Transparency Color Keys*). The Z-order is enabled by setting the DISPC_GFX_ATTRIBUTES[25] ZORDERENABLE bit or the DISPC_VIDp_ATTRIBUTES[25] ZORDERENABLE bit to 0x1 and by defining the Z-order in the DISPC_GFX_ATTRIBUTES[27:26] and DISPC_VIDp_ATTRIBUTES[27:26] ZORDER bit fields. Table 11-112 summarizes the register settings to enable and set the Z-order of a pipeline. Table 11-112 shows the default Z-order values when LCDALPHABLENDERENABLE and ZORDERENABLE are disabled.

Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2943 (highlighted).

The DISPC_GFX_ATTRIBUTES register configures the graphics attributes. Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 3032. In order to be able to set the ZORDER, the window controller obtains data describing the windows in which the graphics images are displayed.

Table 11-244. DISPC_GFX_ATTRIBUTES

Address Offset	0x0000 00A0		
Physical Address	0x5800 10A0	Instance	DISPC
Description	The register configures the graphics attributes. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

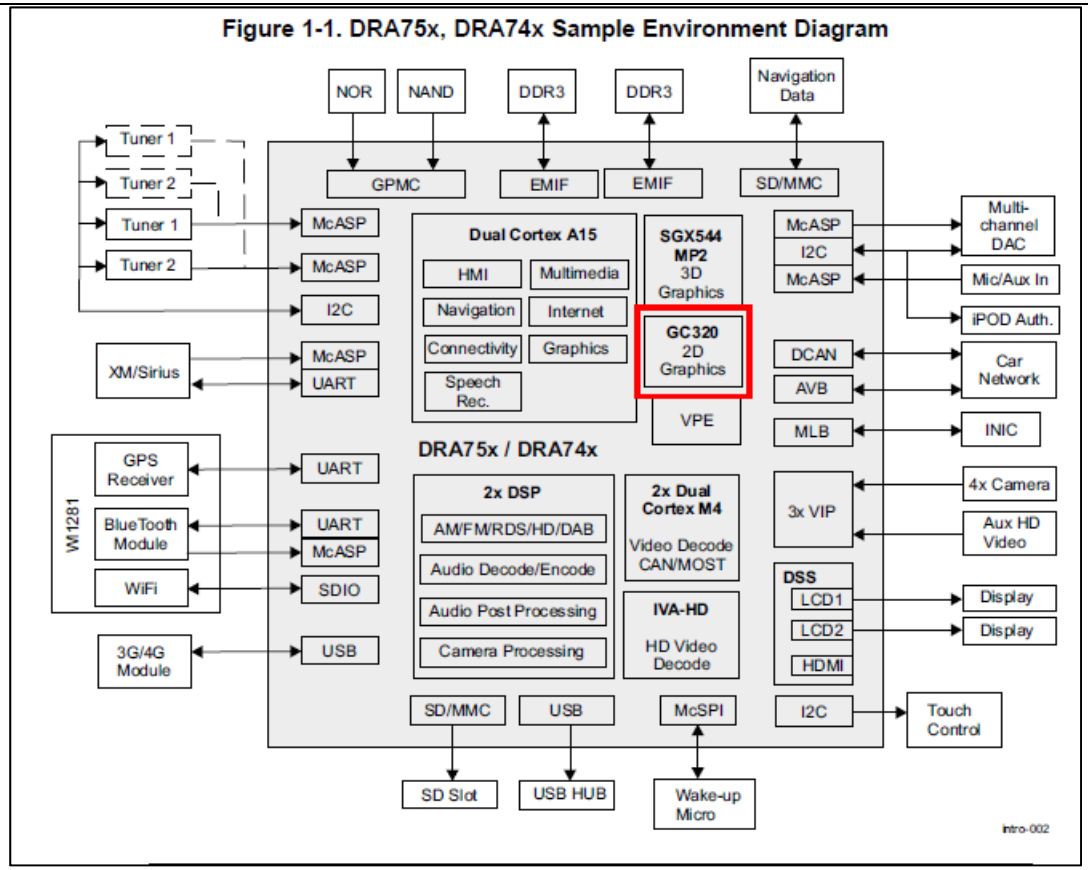
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNELOUT2		BURSTTYPE		PREMULTIPLYALPHA		ZORDER		ZORDERENABLE		ANTIFLICKER		RESERVED		SUBSAMPLINGPATTERN		SELFREFRESHAUTO		FORCE1DTILEDMODE		SELFREFRESH		ARBITRATION		ROTATION		BUFPRELOAD		FRAMEPACKINGMODE		NIBBLEMODE		CHANNELOUT		BURSTSIZE		REPLICATIONENABLE		FORMAT		ENABLE	

***

Bits	Field Name	Description	Type	Reset
27:26	ZORDER	Z-Order defining the priority of the layer compared to others when overlaying. It is software responsibility to ensure that each layer connected to the same overlay manager has a different z-order value. If bit 25 is set to 0, the ZORDER bit field is ignored and replaced by the value 0. 0x0: Z-order 0: layer above solid background color and below layer with higher Z-order values. 0x1: Z-order 1: layer above layer with z-order value of 0 and below layers with z-order values of 2 and 3 0x3: Z-order 3: layer above all the other layers 0x2: Z-order 2: layer above layers with z-order value of 0 and 1 and below layer with z-order value of 3	RW	0x0
25	ZORDERENABLE	Z-order Enable. The bit field ZORDER is only used when the Z-order is enabled. 0x0: Z-order disabled. The Z-order of the layer is 0. 0x1: Z-order enabled. The Z-order is defined by the bit field ZORDER (bits 26 and 27).	RW	0

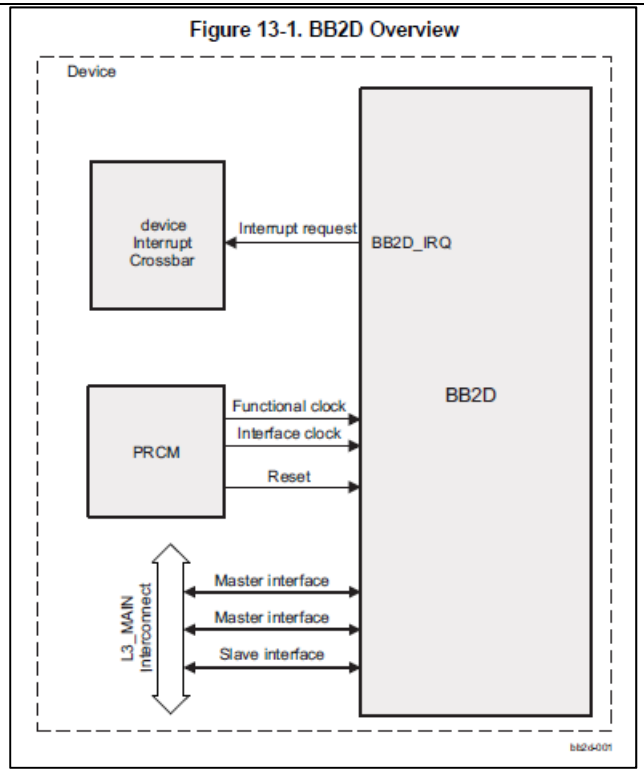
Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Table 11-244 at 3031-32 (highlighted).

Additionally, the Technical Reference Manual for the DRA75x SoC for Automotive Infotainment Silicon Revision 2.0, 1.x discloses that the DRA750 includes a 2D graphics engine, highlighted in red below.

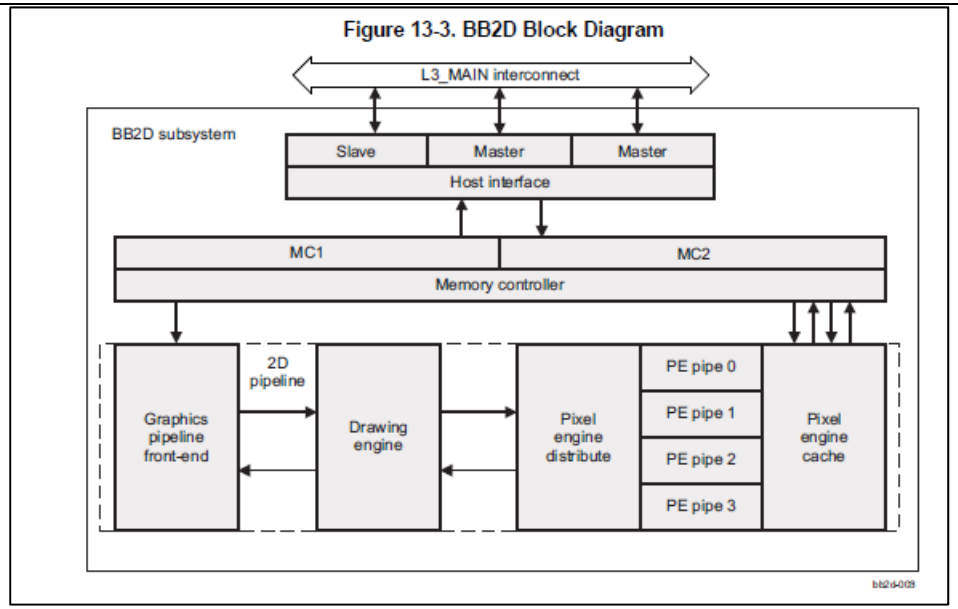


Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Fig. 11-76 at 367 (annotated).

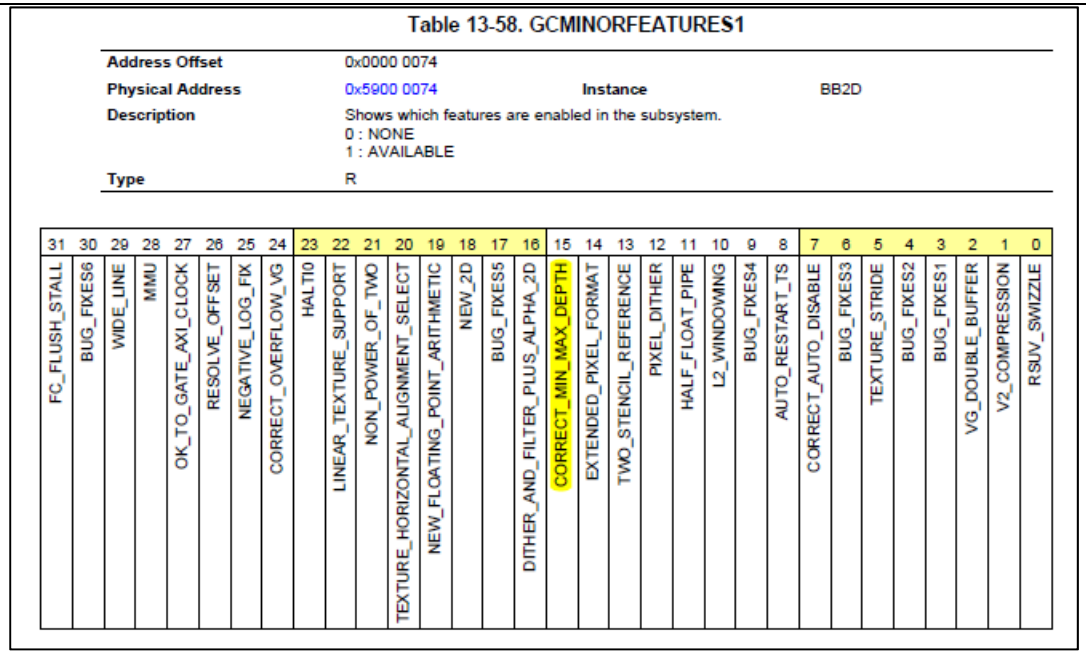
Upon information and belief, the 2D Graphics Engine would access data that describes windows in which the graphics images are displayed and this data would be sorted based on the respective depths of the windows.



Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Fig. 13-1 at 3195.

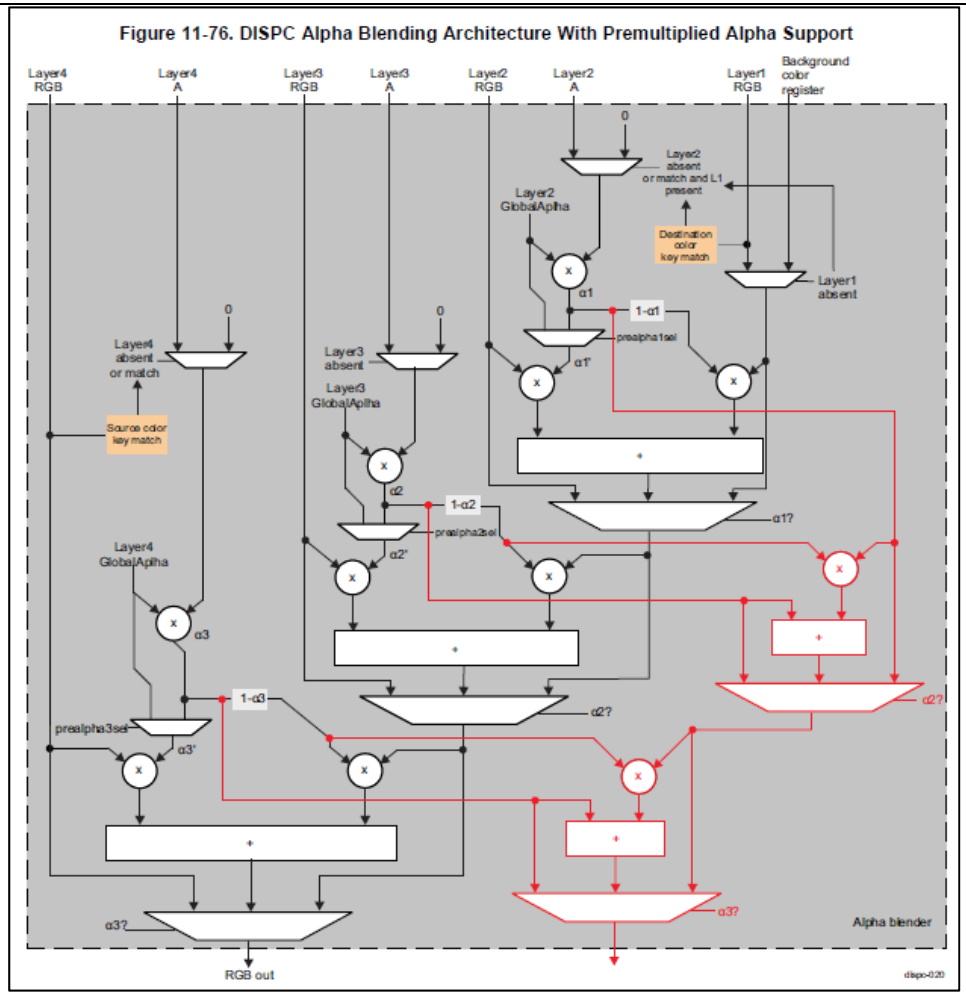


Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Fig. 13-1 at 3199.

<table>
<tr>
<td></td>
<td>


Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Fig. 13-1 at 3216 (highlighted).
</td>
</tr>
<tr>
<td>a display engine for blending the graphics images using alpha values associated with the graphics images; and</td>
<td>The Accused Texas Instrument Infotainment SoCs’ and head units and automobiles that incorporate the Accused Texas Instrument Infotainment SoCs’ system for processing graphics images comprises a display engine for blending the graphics images using alpha values associated with the graphics images.

For example, the Technical Reference Manual for the DRA75x SoC for Automotive Infotainment Silicon Revision 2.0, 1.x discloses that the Display Controller includes an alpha blender, as shown below.</td>
</tr>
</table>



Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Fig. 11-76 at 2946.

Additionally, the Technical Reference Manual explains that once the windows are configured based on their Z-order, alpha blending factors are used to blend the layers together.

11.2.4.13.1.1 DISPC Priority Rule

The overlay manager is configured using the Z-order parameter. The Z-order value defined for each pipeline indicates the visibility order to the window on the screen. If the Z-order value of window A is lower than the Z-order to layer B, layer A is displayed below layer B. The transparency color keys and the alpha blending factors are then used to blend the layers together (see Section 11.2.4.13.1.2, *DISPC ALPHA Blender*, and Section 11.2.4.13.1.3, *DISPC Transparency Color Keys*). The Z-order is enabled by setting the DISPC_GFX_ATTRIBUTES[25] ZORDERENABLE bit or the DISPC_VIDp_ATTRIBUTES[25] ZORDERENABLE bit to 0x1 and by defining the Z-order in the DISPC_GFX_ATTRIBUTES[27:26] and DISPC_VIDp_ATTRIBUTES[27:26] ZORDER bit fields. Table 11-112 summarizes the register settings to enable and set the Z-order of a pipeline. Table 11-112 shows the default Z-order values when LCDALPHABLENDERENABLE and ZORDERENABLE are disabled.

Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2943; *see also* 2946-47 (highlighted).

The Technical Reference Manual for the DRA75x SoC for Automotive Infotainment Silicon Revision 2.0, 1.x also explains that the 2D Graphics Engine blends the graphics images using alpha values.

13.1.1 BB2D Key Features Overview

- API support:
  - OpenWF™, DirectFB
  - GDI/DirectDraw™
  - Flash
- **BB2D architecture:**
  - BitBlt and StretchBlt
  - DirectFB hardware acceleration
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Clipping rectangle support
  - Alpha blending includes Java® 2 Porter-Duff compositing rules
  - 90-, 180-, 270-degree rotation on every primitive
  - YUV-to-RGB color space conversion

Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 3195 (highlighted).

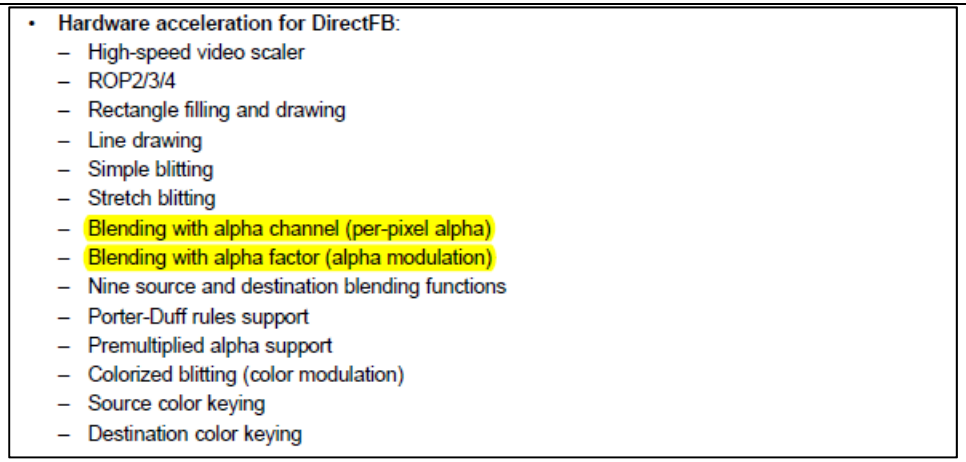
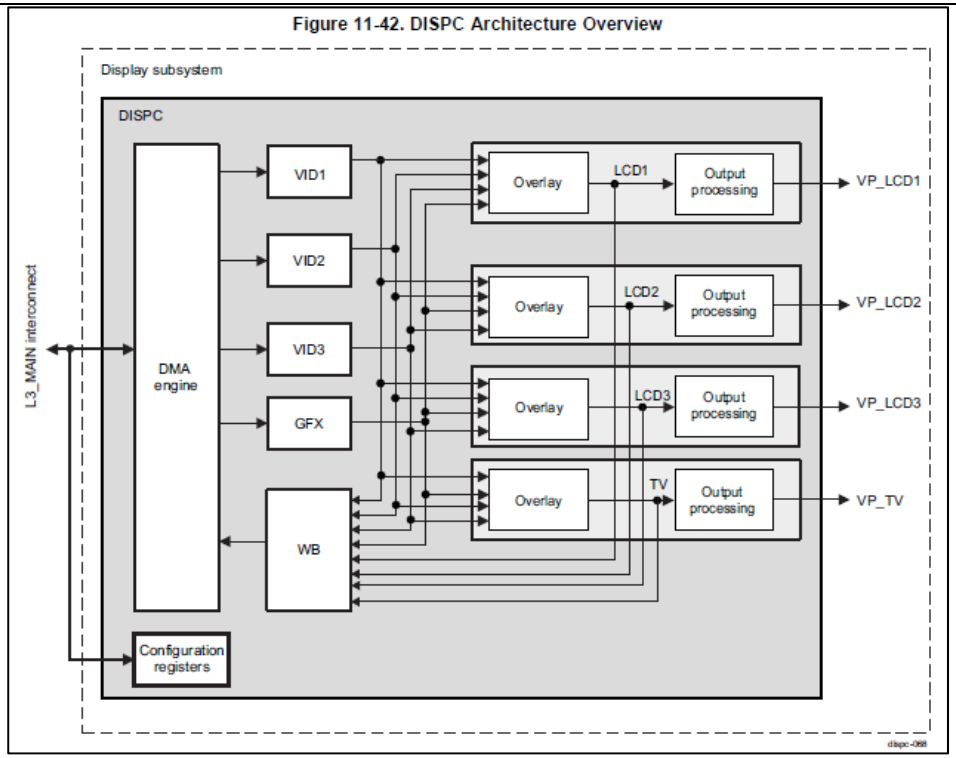
	 Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 3196 (highlighted).
a memory for storing the graphics images,	The Accused Texas Instrument Infotainment SoCs' and head units and automobiles that incorporate the Accused Texas Instrument Infotainment SoCs' system for processing graphics images comprises a memory for storing the graphics images. For example, the Technical Reference Manual for the DRA75x SoC for Automotive Infotainment Silicon Revision 2.0, 1.x explains that "[t]he DISPC can read and display the encoded pixel data stored in memory and write the output of one of the overlays or one of the pipelines into system memory." Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2900. The DISPC architecture is shown below.

Figure 11-42. DISPC Architecture Overview



Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Fig. 11-42, at 2900

In the DISPC, the DMA engine supplies the data from the memories to the graphics and video processing pipelines and stores encoded pixel data to the memories through the WB pipeline.

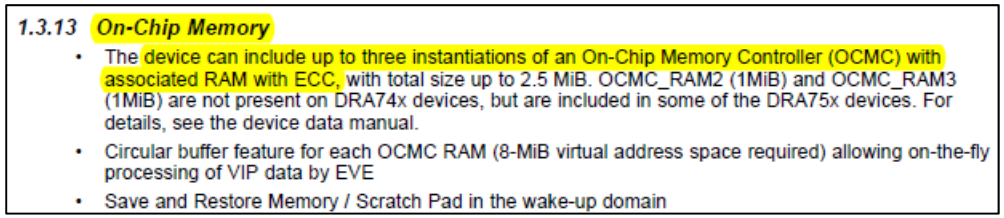
11.2.4.6 DISPC DMA Engine

The DMA engine:

- Supplies data (encoded pixel data and gamma curve) from memories to the GFX, VID1, VID2, and VID3 pipelines through the interconnect based on the configuration of the DISPC and pipeline setting.
- Stores encoded pixel data from GFX/VID pipelines or overlays to memories through the WB pipeline and interconnect based on the configuration of the DISPC and WB pipeline setting.

Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2905 (highlighted).

The Technical Reference Manual explains that the DRA75x SoC also includes on-chip memory.

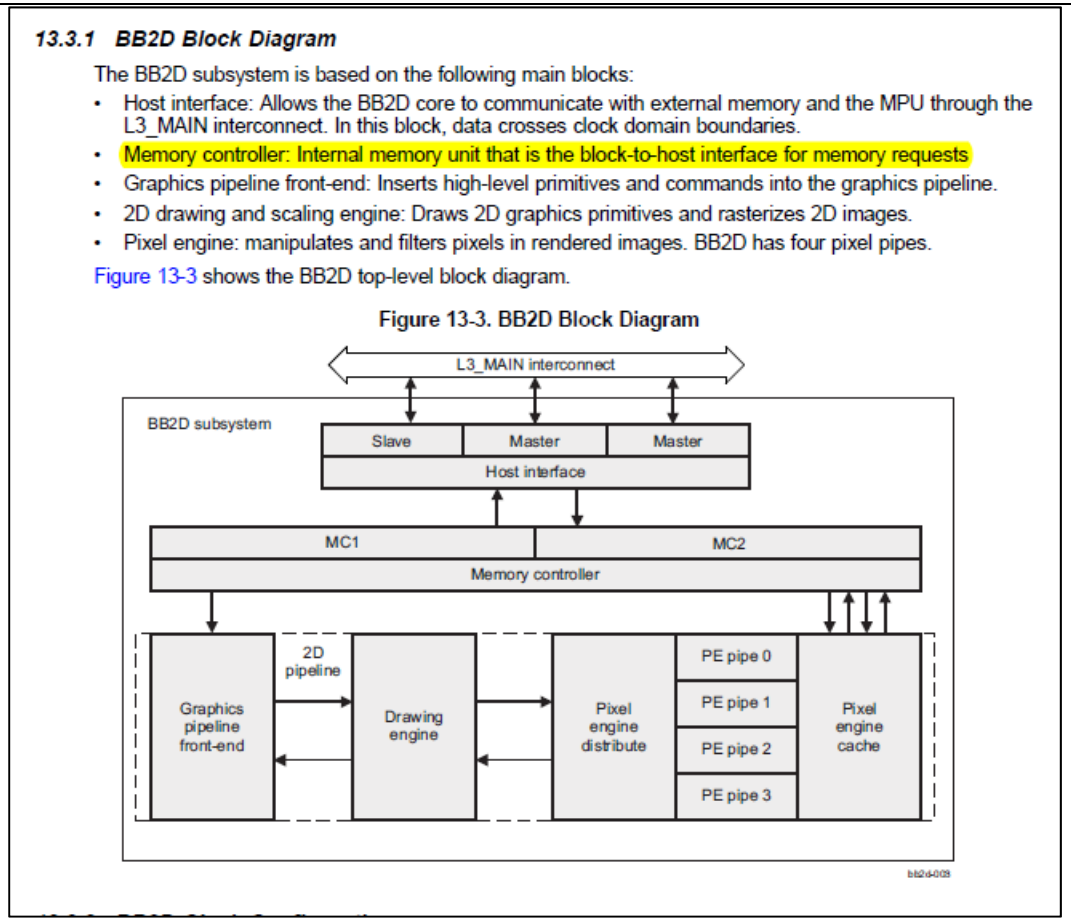


1.3.13 On-Chip Memory

- The device can include up to three instantiations of an On-Chip Memory Controller (OCMC) with associated RAM with ECC, with total size up to 2.5 MiB. OCMC_RAM2 (1MiB) and OCMC_RAM3 (1MiB) are not present on DRA74x devices, but are included in some of the DRA75x devices. For details, see the device data manual.
- Circular buffer feature for each OCMC RAM (8-MiB virtual address space required) allowing on-the-fly processing of VIP data by EVE
- Save and Restore Memory / Scratch Pad in the wake-up domain

Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 373 (highlighted).

The Technical Reference Manual for the DRA75x SoC for Automotive Infotainment Silicon Revision 2.0, 1.x also explains that the 2D Graphics Engine includes a memory controller and can communicate with external memory and the MPU. Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 3199.



13.3.1 BB2D Block Diagram

The BB2D subsystem is based on the following main blocks:

- Host interface: Allows the BB2D core to communicate with external memory and the MPU through the L3_MAIN interconnect. In this block, data crosses clock domain boundaries.
- Memory controller: Internal memory unit that is the block-to-host interface for memory requests
- Graphics pipeline front-end: Inserts high-level primitives and commands into the graphics pipeline.
- 2D drawing and scaling engine: Draws 2D graphics primitives and rasterizes 2D images.
- Pixel engine: manipulates and filters pixels in rendered images. BB2D has four pixel pipes.

Figure 13-3 shows the BB2D top-level block diagram.

Figure 13-3. BB2D Block Diagram

Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Fig. 11-42, at 3199 (highlighted).

wherein the window controller transmits header packets to the display engine, each header packet containing at least a portion of the	The Accused Texas Instrument Infotainment SoCs' and head units and automobiles that incorporate the Accused Texas Instrument Infotainment SoCs' window controller transmits header packets to the display engine, each header packet containing at least a portion of the data, said portion describing at least one of the windows. In the operation of at least the Display Controller (DISPC) and the 2D Graphics Engine (BB2D), the

data, said portion describing at least one of the windows, and	window controller transmits header packets containing data describing the windows. For example, in the DISPC, the height and width of each enabled layer as well as the position of the pixels is defined by the setting of certain bits in registers.

The height and width of each enabled layer (pipeline) must be defined in the SIZEY and SIZEX bit fields DISPC_GFX_SIZE[27:16][10:0]/ DISPC_VIDp_SIZE[27:16][10:0], and its x and y positions defined in the POSX and POSY bit fields DISPC_GFX_POSITION[26:16][10:0]/DISPC_VIDp_POSITION[26:16][10:0]. If there are no graphics or video-encoded pixels at a specific position, the programmable, solid background color appears. The solid background color is set in the DISPC_DEFAULT_COLORo[23:0] DEFAULTCOLOR bit field. Figure 11-75 is an example of priority rule.

Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2945 (highlighted).

Table 11-242. DISPC_GFX_SIZE

Address Offset	0x0000 008C		
Physical Address	0x5800 108C	**Instance**	DISPC
Description	The register configures the size of the graphics window. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	SIZEY	RESERVED	SIZEX

Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 3031 (highlighted).

Table 11-240. DISPC_GFX_POSITION

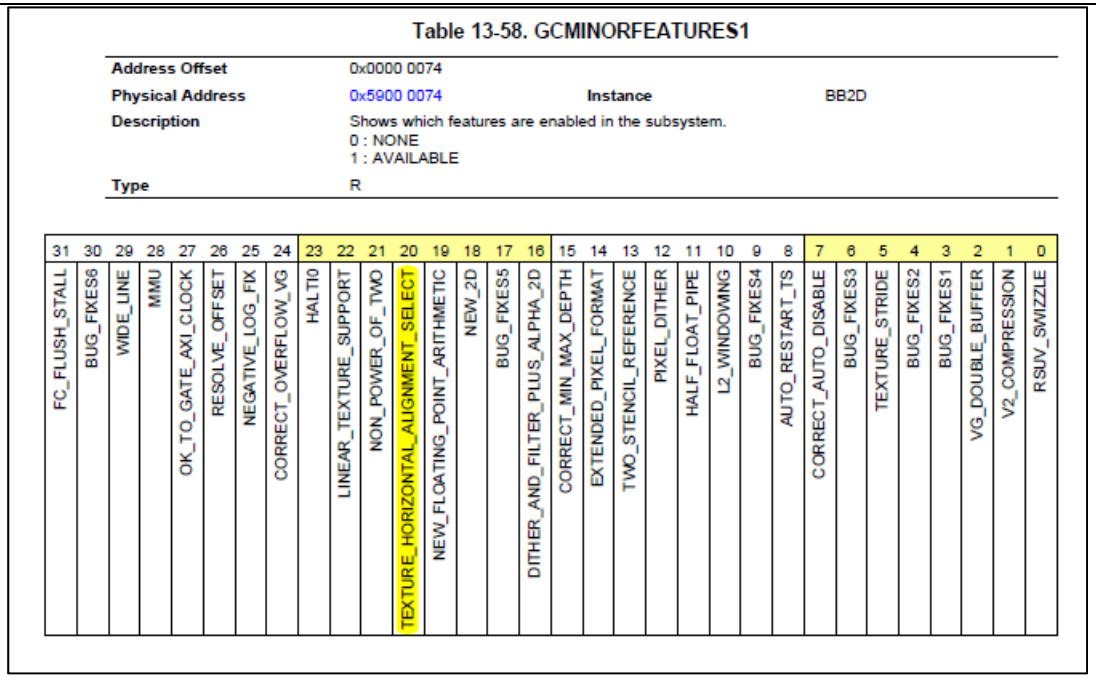
Address Offset	0x0000 0088
Physical Address	0x5800 1088 **Instance** DISPC
Description	The register configures the position of the graphics window. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or VFP start period of the third LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, third LCD, TV output or write-back to the memory
Type	RW

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	POSY	RESERVED	POSX

Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
26:16	POSY	Y position of the graphics window. Encoded value (from 0 to 2047) to specify the Y position of the graphics window on the screen. The line at the top has the Y-position 0.	RW	0x000
15:11	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0x00
10:0	POSX	X position of the graphics window. Encoded value (from 0 to 2047) to specify the X position of the graphics window on the screen. The first pixel on the left of the screen has the X-position 0.	RW	0x000

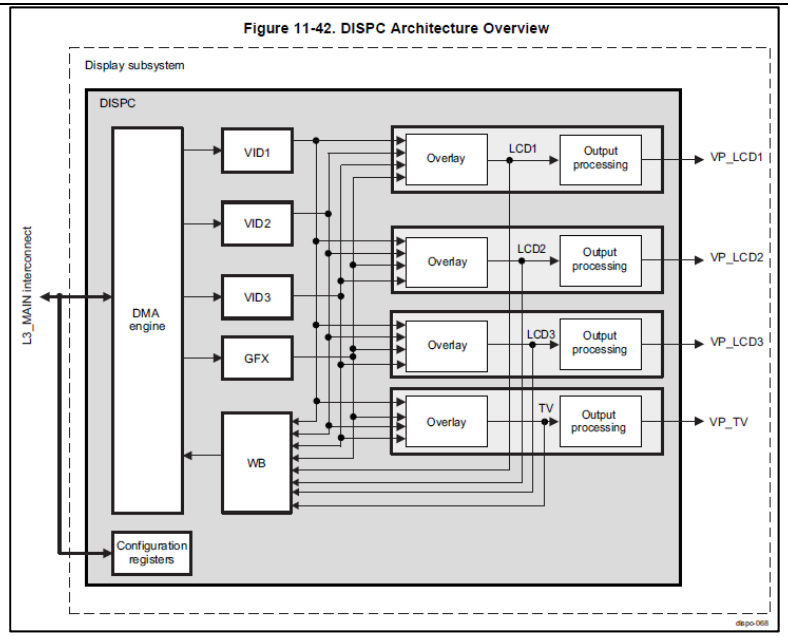
Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 3031 (highlighted).

Additionally, in the 2D Graphics Engine, upon information and belief, the setting of certain bits in certain registers describes aspects of at least one of the windows, such as the alignment of the window.

<table>
<tr>
<td></td>
<td>


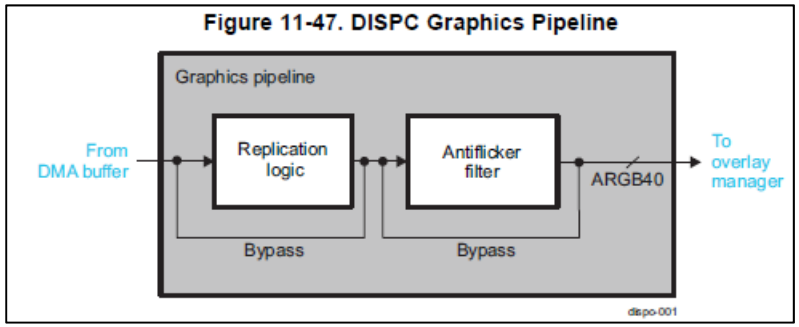
Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 3216 (highlighted).
</td>
</tr>
<tr>
<td>wherein the graphics images are transferred from the memory to the display engine responsive to said header packets.</td>
<td>The Accused Texas Instrument Infotainment SoCs’ and head units and automobiles that incorporate the Accused Texas Instrument Infotainment SoCs’ transfer graphics images from the memory to the display engine responsive to said header packets.

For example, the Technical Reference Manual for the DRA75x SoC for Automotive Infotainment Silicon Revision 2.0, 1.x explains that “[t]he DISPC can read and display the encoded pixel data stored in memory and write the output of one of the overlays or one of the pipelines into system memory.” Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2900. The Technical Reference Manual also explains that “[a]n overlay manager manages inputs of multiple pipelines.” Id.</td>
</tr>
</table>



Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Fig. 11-42 at 2900

The Technical Reference Manual further explains that, as shown below, the graphics entering the graphics pipeline come from the DMA buffer and then lead to the overlay manager.



Ex. 65 - DRA75x, DRA74x Technical Reference Manual, Fig. 11-47 at 2919

	Additionally, the Technical Reference Manual explains that the DISPC overlay optimization fetches only the required pixels from the memory and that this selection is based on registers, which were set in accordance with the header packets. *11.2.4.13.1.4 DISPC Overlay Optimization* The overlay optimization consists in fetching only the required pixels (that is, pixels that contribute to the final picture to be displayed [LCD1, LCD2, LCD3, or TV]). The decision to fetch the pixel from memory is based on the information available in the registers and on the following rules: • The layer is enabled. • The global alpha blending factor for the layer is different than 0x00. • The current layer is behind an nonopaque layer (global alpha blending factor is different than 0xFF for the layer in the preceding). The result of the overlay optimization is a reduction of the bandwidth by fetching only the mandatory pixels. The overlay mechanism is independent for each overlay: LCD1, LCD2, LCD3, and TV. Because each layer (GFX, VID1, VID2, and VID3) can be associated to only one overlay at a time, it is possible to optimize the fetch of the pixels for each layer based on the overlay information. The overlay optimization must be run on the DMA engine time window and not on the display time window. The pixels are fetched by the DMA engine before the display processing. Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 2950 (highlighted). With respect to the 2D Graphics Engine, the Technical Reference Manual explains that the BB2D includes a memory controller that is the "block-to-host interface for memory requests." Ex. 65 (Tech Ref Manual) at 3199. As can be seen in the Figure below, both the Graphics Pipeline front-end and pixel engine cache communicate with the memory controller.

13.3 BB2D Functional Description

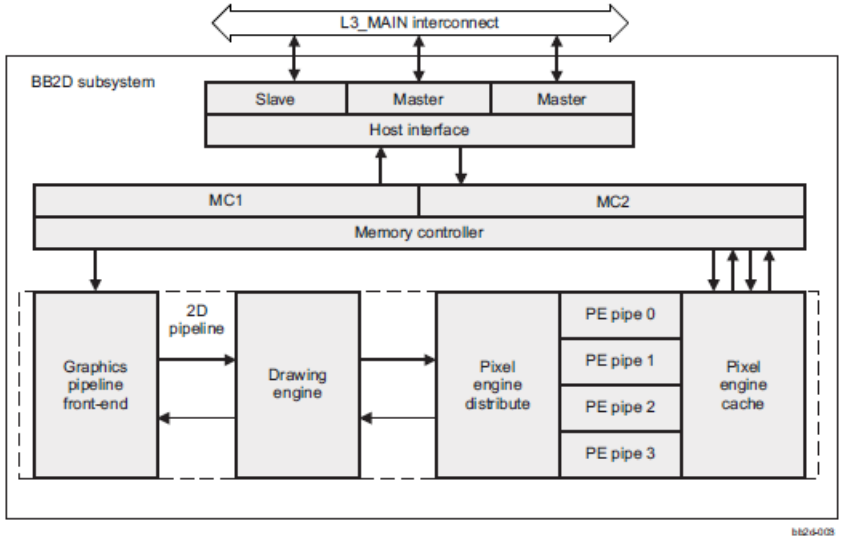
13.3.1 BB2D Block Diagram

The BB2D subsystem is based on the following main blocks:

- Host interface: Allows the BB2D core to communicate with external memory and the MPU through the L3_MAIN interconnect. In this block, data crosses clock domain boundaries.
- Memory controller: Internal memory unit that is the block-to-host interface for memory requests
- Graphics pipeline front-end: Inserts high-level primitives and commands into the graphics pipeline.
- 2D drawing and scaling engine: Draws 2D graphics primitives and rasterizes 2D images.
- Pixel engine: manipulates and filters pixels in rendered images. BB2D has four pixel pipes.

Figure 13-3 shows the BB2D top-level block diagram.

Figure 13-3. BB2D Block Diagram



Ex. 65 - DRA75x, DRA74x Technical Reference Manual at 3199 (highlighted).